High Current Driver Amplifier and Digital VGA/Preamplifier with 3 dB Steps

Preliminary Technical Data

AD8260

FEATURES

Driver amplifier
- **Differential configuration—direct drive from DAC**
- **Preset gain of 1.5×**
- **3 dB bandwidth: 155 MHz**
- **Large output drive: >±300 mA**

Combined preamplifier and VGA
- **Low noise**
  - **Voltage noise: 2.4 nV/√Hz**
  - **Current noise: 5 pA/√Hz**
- **−3 dB bandwidth: 180 MHz**
- **Gain range: 30 dB in 3 dB steps**
  - **−6 dB to +24 dB (preamplifier gain = 6 dB)**
- **Single-ended preamplifier input and differential output**

Supplies: 3.3 V to 10 V (with VMID enabled)
- **±3.3 V to ±5 V (with VMID disabled)**

Power: 93 mW with 3.3 V supplies
- **Power-down for VGA, driver amplifier, and system**

FUNCTIONAL BLOCK DIAGRAM

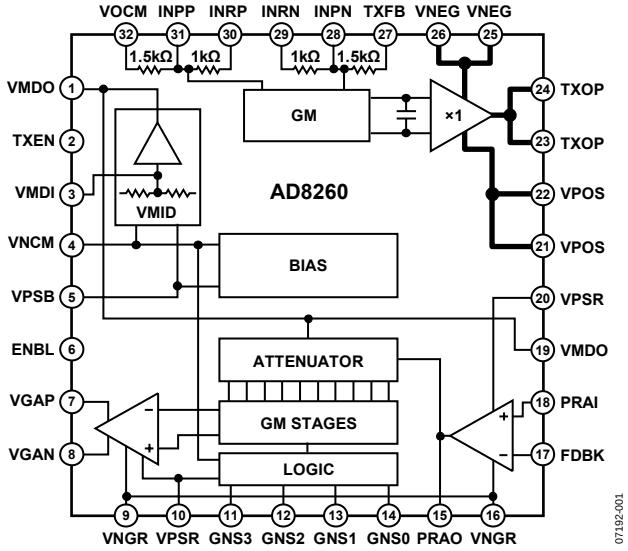


Figure 1. Functional Block Diagram

APPLICATIONS

Digital AGC systems
Tx/Rx signal processing
Power-line transceivers

GENERAL DESCRIPTION

The AD8260 includes a high current driver, usable as a transmitter, and a low noise, digitally programmable variable gain amplifier (DGA), useable as a receiver, combined in a 5 mm × 5 mm, 32-lead chip scale package.

The receiver section consists of a single-ended input preamplifier, and linear-in-dB, differential-output VGA. Usable at dc and frequencies to 80 MHz; the –3 dB bandwidth is 180 MHz. The driver-amplifier delivers ±300 mA, well suited for driving low impedance loads, even when connected to a 3.3 V supply.

The AD8260 DGA is ideal for trim applications and has a gain span of 30 dB, in 3 dB steps. Excellent bandwidth uniformity is maintained across the entire frequency range. The DGA's low output-referred noise is advantageous in driving high speed ADCs. The differential output facilitates the interface to modern low voltage high speed ADCs.

Single-supply and dual-supply operation makes the part versatile and enables gain control of negative-going pulses, such as generated by photodiodes or photo-multiplier tubes, as well as processing band-pass signals on a single supply. For maximum dynamic range, it is essential that the part be ac-coupled when operating on a single supply.

The AD8260 preamplifier (PrA) is user configurable with external resistors for gains greater than 6 dB; as with any high frequency op amp, the gain is inverting or noninverting. The DGA is characterized with a noninverting PrA gain of 2×. The attenuator has a range of 30 dB and the output amplifier has a gain of 8× (18.06 dB). The lowest noninverting gain range is −6 dB to +24 dB and shifts up with increased PrA gain. The gain is controlled via a parallel port (Pin GNS0 to Pin GNS3) with 10 gain steps of 3 dB per code. For any nonused code, the preamplifier and DGA are disabled.

The AD8260 can operate with single or dual supplies from 3.3 V to ±5 V. An internal buffer normally provides a split supply reference for single-supply operation; an external reference can also be used when the VMID buffer is shut down.

The operating temperature range is −40°C to +105°C. The AD8260 is available in a 32-lead LFCSP.

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Revision History ..... **Error! Bookmark not defined.**
Specifications 3
Absolute Maximum Ratings 6
ESD Caution 6
Pin Configuration and Function Descriptions 7
Typical Performanance Characteristics 8
Theory of Operation 16
Introduction 16
High Current Driver Amplifier 17
Precautions to be Observed During Design 17
VMID Buffer 17
Preamplifier 17
Preamplifier Noise 17
DGA 18
Gain Control 18
Output Stage 18
Attenuator 18
Single-Supply Operation and AC Coupling 18
Power Up/Down Sequence 19
Logic Interfaces 19
Outline Dimensions 20
Ordering Guide 20

SPECIFICATIONS

V_S = 3.3 V, T_A = 25°C, PrA gain = +2 (R_{FB1} = R_{FB2} = 100 Ω), V_{VMDO} = V_S/2; f = 10 MHz, C_L = 5 pF, R_L = 500 Ω, DGA differential output, all dBm referenced to 50 Ω, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DRIVER AMPLIFIER—GENERAL PARAMETERS					
–3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p, R_L = 500 Ω				MHz
	V_{OUT} = 10 mV p-p, R_L = 50 Ω				MHz
	V_{OUT} = 10 mV p-p, R_L = 10 Ω				MHz
–3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p				MHz
	V_{OUT} = 2 V p-p				MHz
	V_{OUT} = 2 V p-p, R_L = 50 Ω				MHz
Slew Rate	V_{OUT} = 1 V p-p				V/µs
	V_{OUT} = 2 V p-p				V/µs
	V_{OUT} = 2 V p-p, R_L = 50 Ω				V/µs
Input Voltage Noise	f = 10 MHz				nV/√Hz
Noise Figure	R_S = 100 Ω (differential, 2 × 50 Ω that convert differential DAC output currents to differential voltage)				dB
Output-Referred Noise	Gain = 3.52 dB (1.5×); includes internal gain setting resistors				nV/√Hz
Output Impedance	DC to 10 MHz				Ω
Output Current	R_L = 1 Ω, V_{IN} = ±0.5 V				mA
Output Signal Range	R_L ≥ 500 Ω				V
	V_S = +5 V				V
	V_S = ±5 V				V
Input Signal Range	Differential input signal				Vp-p
Output Offset Voltage	Gain = 3.52 dB (1.5×)				mV
DRIVER AMPLIFIER—DYNAMIC PERFORMANCE					
Harmonic Distortion	V_{OUT} = 1 V p-p				
HD2	f = 1 MHz				dBc
HD3					dBc
HD2	f = 10 MHz				dBc
HD3					dBc
	V_{OUT} = 2 V p-p				
HD2	f = 1 MHz				dBc
HD3					dBc
HD2	f = 10 MHz				dBc
HD3					dBc
Input 1 dB Compression Point					dBm
MTPR (In-Band)	R_L = 50 Ω, V_{OUT} = 1.4 V p-p max, 10 tones, 2 MHz to 22 MHz with missing tone at 12 MHz (spacing 2 MHz)				dBc
	R_L = 50 Ω, V_{OUT} = 1.4 V p-p max, 16 tones, 2 MHz to 38 MHz with missing tones at 10 MHz, 20 MHz, 30 MHz, and 40 MHz (spacing 2 MHz)				dBc
Two-Tone Intermodulation Distortion (IMD3)	V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz				dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz				dBc
	V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz				dBc
	V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz				dBc
Output Third-Order Intercept	V_{OUT} = 1 V p-p, f = 10 MHz				dBm
	V_{OUT} = 2 V p-p, f = 10 MHz				dBm
	V_{OUT} = 1 V p-p, f = 45 MHz				dBm
	V_{OUT} = 2 V p-p, f = 45 MHz				dBm

Parameter	Conditions	Min	Typ	Max	Unit
Two-Tone Intermodulation Distortion (IMD3)	R_L = 50 Ω				dBc
	V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz				
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz				dBc
	V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz				dBc
	V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz				dBc
Output Third-Order Intercept	R_L = 50 Ω				dBm
	V_{OUT} = 1 V p-p, f = 10 MHz				
	V_{OUT} = 2 V p-p, f = 10 MHz				dBm
	V_{OUT} = 1 V p-p, f = 45 MHz				dBm
	V_{OUT} = 2 V p-p, f = 45 MHz				dBm
PRA AND VGA—GENERAL PARAMETERS					
−3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p				MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p				MHz
	V_{OUT} = 2 V p-p				MHz
Slew Rate	V_{OUT} = 1 V p-p				V/µs
	V_{OUT} = 2 V p-p				V/µs
Input Voltage Noise	f = 10 MHz (input short)				nV/√Hz
	f = 10 MHz (input open)				nV/√Hz
Noise Figure	Max gain (code = 1011), R_S = 50 Ω, unterminated				dB
	Max gain (code = 1011), R_S = 50 Ω, shunt terminated with 50 Ω				dB
Output-Referred Noise	Max gain (code = 1011), gain = 24 dB (input short)				nV/√Hz
	Max gain (code = 1011), gain = 24 dB (input open)				nV/√Hz
	Min gain (code = 0001), gain = −6 dB				nV/√Hz
Output Impedance	DC to 10 MHz				Ω
Output Signal Range (per pin)	R_L ≥ 500 Ω				V
	V_S = +5 V				V
	V_S = ±5 V				V
Input Signal Range	Preamplifier input				V
Output Offset Voltage	Max gain (code = 1011), gain = 30 dB				mV
PRA AND VGA—DYNAMIC PERFORMANCE					
Harmonic Distortion	Code = 0110, gain = 9 dB, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz				dBc
HD3					dBc
HD2	f = 10 MHz				dBc
HD3					dBc
	Code = 1011, gain = 24 dB, V_{OUT} = 2 V p-p				
HD2	f = 1 MHz				dBc
HD3					dBc
HD2	f = 10 MHz				dBc
HD3					dBc
Input 1 dB Compression Point	Min gain (code = 0001), gain = −6 dB, (preamplifier limited)				dBm
	Max gain (code = 1011), gain = 24 dB, (VGA limited)				dBm
MTPR (In-Band)	V_{OUT} = 1.4 V p-p max, 10 tones, 2 MHz to 22 MHz with missing tone at 12 MHz (spacing 2 MHz); code = 1011, gain = 24 dB				dBc
	V_{OUT} = 1.4 V p-p max, 16 tones, 2 MHz to 38 MHz with missing tones at 10 MHz, 20 MHz, 30 MHz, and 40 MHz (spacing 2 MHz)				dBc

Parameter	Conditions	Min	Typ	Max	Unit
Two-Tone Intermodulation Distortion (IMD3)	Code = 1011, gain = 24 dB				
	V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz				dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz				dBc
	V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz				dBc
	V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz				dBc
Output Third-Order Intercept	Code = 1011, gain = 24 dB				
	V_{OUT} = 1 V p-p, f = 10 MHz				dBm
	V_{OUT} = 2 V p-p, f = 10 MHz				dBm
	V_{OUT} = 1 V p-p, f = 45 MHz				dBm
	V_{OUT} = 2 V p-p, f = 45 MHz				dBm
Overload Recovery	Max gain (code = 1011), gain = 24 dB, V_{IN} = 50 V p-p to 500 mV p-p				ns
Group Delay Variation	1 MHz < f < 50 MHz, full gain range				ns
ACCURACY					
Absolute Gain Error	All codes				dB
Gain Law Conformance (DNL)	Differential gain error code-to-code				dB
GAIN CONTROL					
Gain Step per Code					dB
Gain Range					dB
Response Time	30 dB gain change (code stepped from 0001 to 1011)				ns
LOGIC INTERFACES					
High Level Input Voltage		1.4		V_S	V
Low Level Input Voltage		0		0.8	V
Logic Input Bias Current	Logic high, V_{LOGIC} = 3.3 V				nA
	Logic low				nA
POWER SUPPLY					
Supply Voltage	$V_{POS} - V_{NEG}$ (dual or single-supply)	|3.3|		|10|	V
Quiescent Current	Full chip enabled (TXEN = 1, ENBL = 1, code = 0001)				mA
	TXEN = 0, ENBL = 1, code = 0001, driver off, DGA on				mA
	TXEN = 1, ENBL = 1, code = 0000, driver on, DGA off				mA
	Chip disabled (TXEN = 0, ENBL = 0, code = 0000)				µA
	V_S = ±5 V, no signal				mA
PSRR	Max gain (code = 1011), gain = 30 dB, 1 MHz				dB
	Driver amplifier, 1 MHz				dB
Power Dissipation	No signal				mW
	No signal, $V_{POS} - V_{NEG}$ = 10 V				mW
ENABLE TIMES					
Chip Enable Time	Bias only, TXEN = 0, code = 0000, ENBL = 0 to 1				µs
	All at once, TXEN = 0 to 1, code = 0000 to 0001, ENBL = 0 to 1				µs
PrA + DGA Enable Time	ENBL = 1, TXEN = 0, code = 0000 to 0001				µs
Driver Enable Time	ENBL = 1, code = 0001, TXEN stepped from 0 to 1				µs
DISABLE TIMES					
Chip Disable Time	TXEN = 1 to 0, code = 0001 to 0000, ENBL = 1 to 0 for I_S = 100 µA				µs
	All at once; TXEN = 1 to 0 , code = 0001 to 0000, ENBL = 1 to 0 for I_S = 35 µA V_S				µs
PrA + DGA Disable Time	ENBL = 1, TXEN = 0, code = 0001 to 0000				µs
Driver Disable Time	ENBL = 1, code = 0000, TXEN = 1 to 0				µs

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	±6 V
Input Voltage (INxx, PRAI, FDBK, VMDI, VOCM)	VPOS, VNEG
Logic Voltages	VPOS, Ground
Power Dissipation	TBD W
Temperature	
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Thermal Data	
θ_{JA}	TBD °C/W
θ_{JC}	TBD °C/W
Ψ_{JT}	TBD °C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

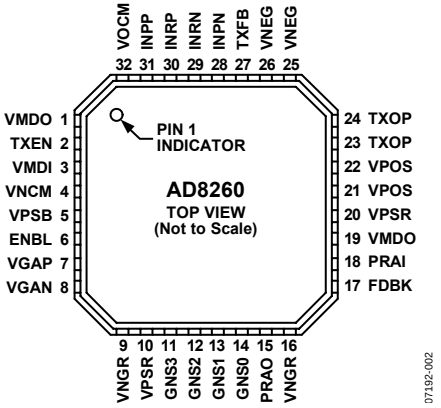


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VMDO	VMID Buffer Output. Normally decoupled with a 0.1 µF capacitor.
2	TXEN	Driver Enable. Logic threshold = 1.1 V with ±0.2 V hysteresis.
3	VMDI	VMID Input Voltage. Normally decoupled with a 0.1 µF capacitor. When pulled to VNCM, the VMID buffer shuts down. This can be useful when using the part with dual supplies or when an external midpoint generator is used.
4	VNCM	Negative Supply for Bias Cell, VMID Cell, and Logic Inputs. (Ground this pin in applications.)
5	VPSB	Positive Supply for Bias Cell and VMID Cell.
6	ENBL	Chip Enable. Logic threshold = 1.1 V. When low, the current consumed is only 28 µA.
7	VGAP	Positive VGA Output. (Needs to be ac-coupled for single supply).
8	VGAN	Negative VGA Output. (Needs to be ac-coupled for single supply).
9	VNGR	Negative Supply for PrA and DGA (–VPOS for Dual Supply; GND for Single Supply).
10	VPSR	Positive Supply for PrA, DGA, and GNSx Logic Decoder.
11	GNS3	MSB for Gain Control. Logic threshold = 1.1 V.
12	GNS2	Gain Control Bit. Logic threshold = 1.1 V.
13	GNS1	Gain Control Bit. Logic threshold = 1.1 V.
14	GNS0	LSB for Gain Control. Logic threshold = 1.1 V.
15	PRAO	Preamplifier Output.
16	VNGR	Negative Supply for PrA and DGA (–VPOS for Dual Supply; GND for Single Supply).
17	FDBK	Negative Input of Preamplifier.
18	PRAI	Positive Input of Preamplifier.
19	VMDO	VMID Buffer Output. Normally decoupled with at least a 0.1 µF capacitor.
20	VPSR	Positive Supply for PrA, DGA, and GNSx Logic Decoder.
21	VPOS	Positive Supply for Driver Amplifier.
22	VPOS	Positive Supply for Driver Amplifier.
23	TXOP	Driver Output.
24	TXOP	Driver Output.
25	VNEG	Negative Supply for Driver Amplifier (–VPOS for Dual Supply; GND for Single Supply).
26	VNEG	Negative Supply for Driver Amplifier (–VPOS for Dual Supply; GND for Single Supply).
27	TXFB	Feedback for Driver Amplifier.
28	INPN	Negative Driver Amplifier Input.
29	INRN	Negative Gain Resistor Input for Driver Amplifier.
30	INRP	Positive Gain Resistor Input for Driver Amplifier.
31	INPP	Positive Driver Amplifier Input.
32	VOCM	Output Common Mode Pin; Normally Connected to Pin VMDO.

TYPICAL PERFORMANANCE CHARACTERISTICS

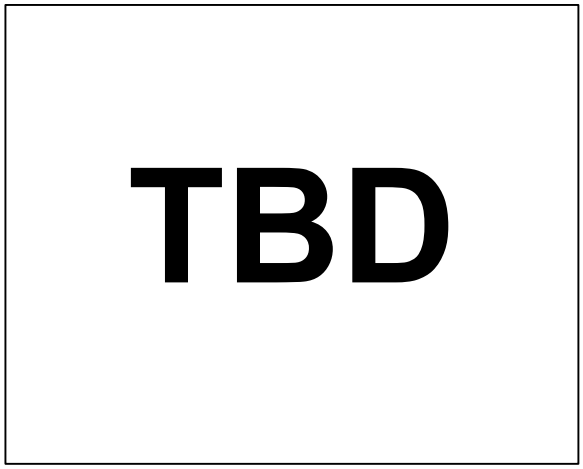
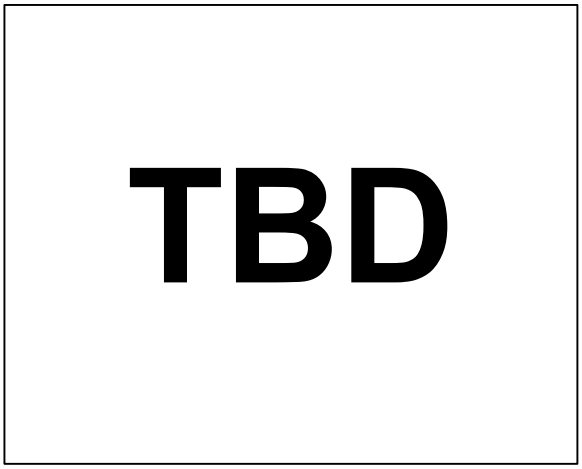


Figure 3.



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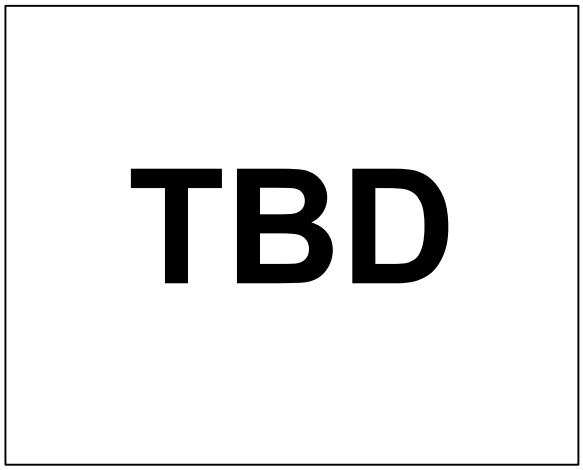

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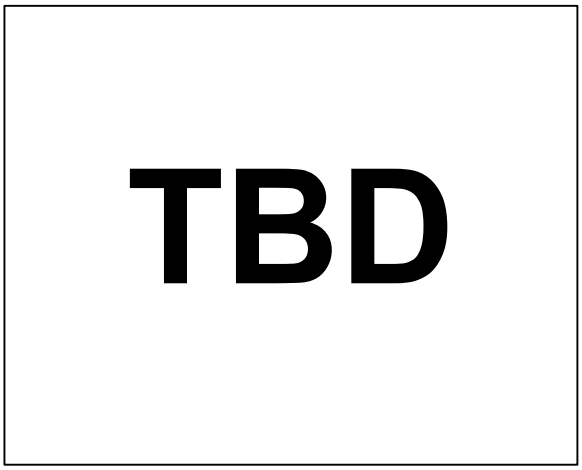

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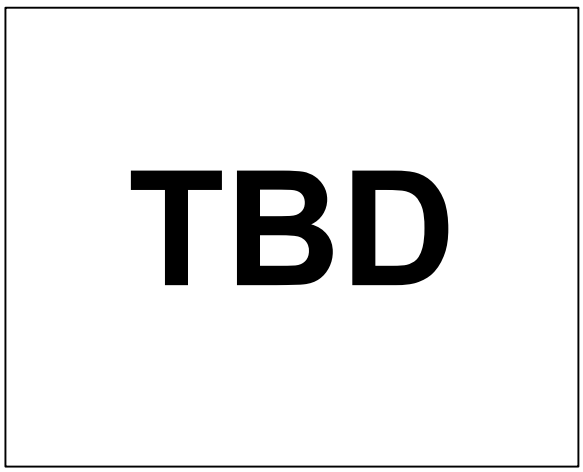
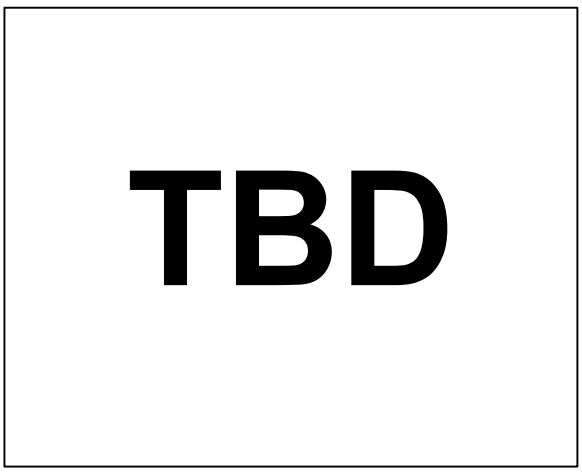


Figure 5.



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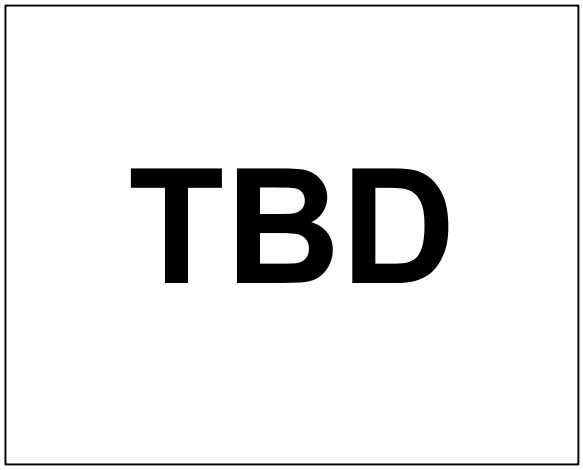

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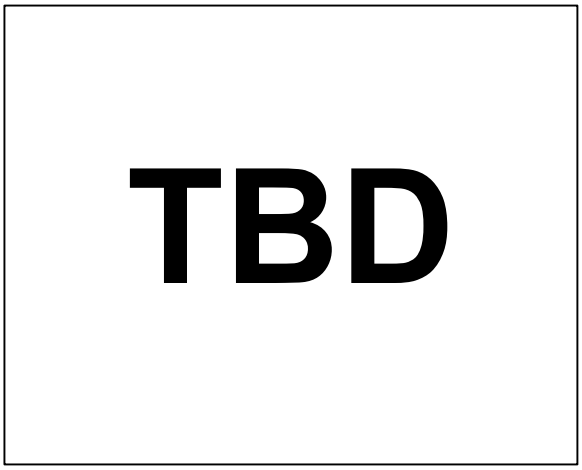

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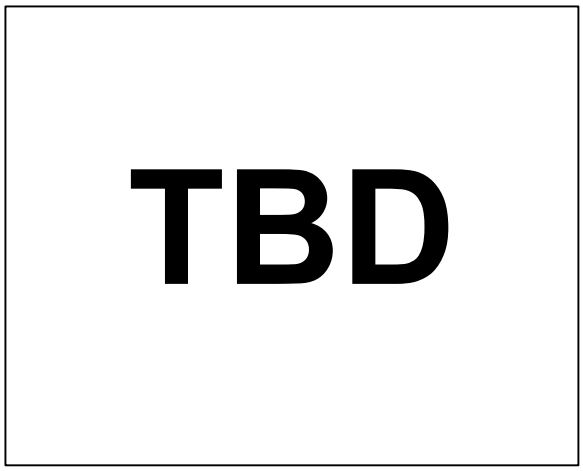

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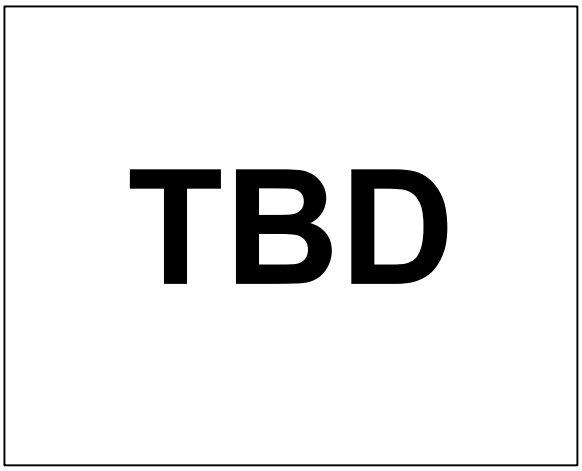

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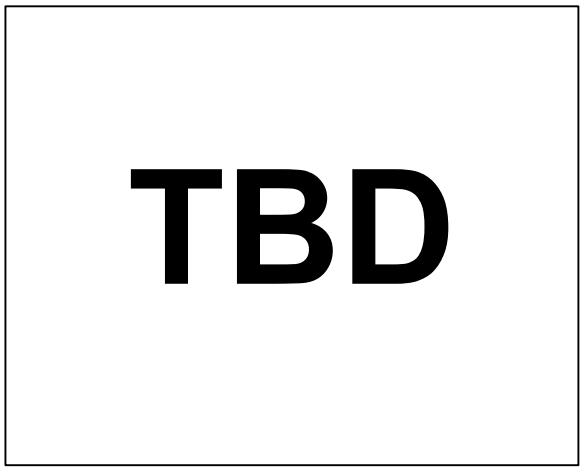

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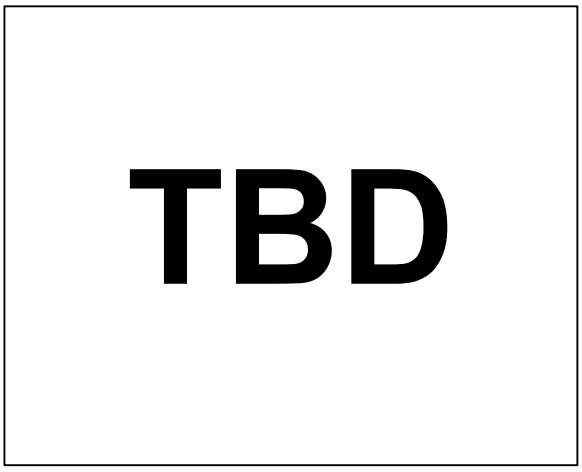

Figure 14.

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Figure 15.

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Figure 16.

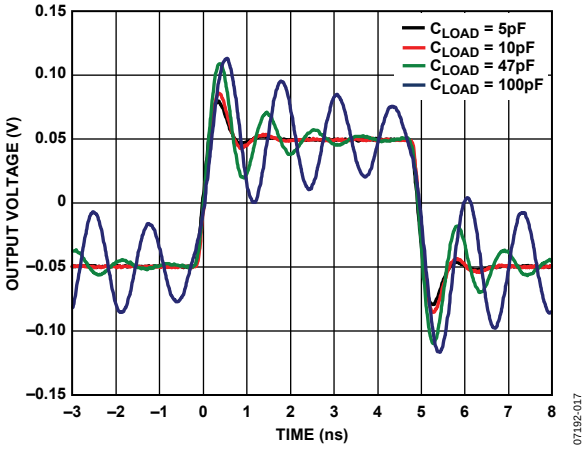


Figure 17. Small Signal Pulse Response for Various Values of Load Capacitance C_{LOAD}

TBD

Figure 18.

TBD

Figure 19.

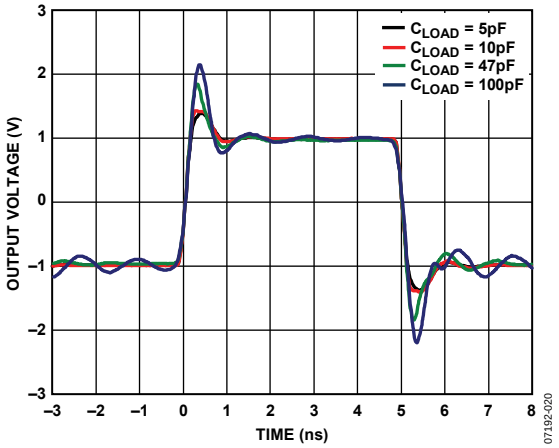


Figure 20. Large Signal Pulse Response for Various Values of Load Capacitance C_{LOAD}

TBD

Figure 21

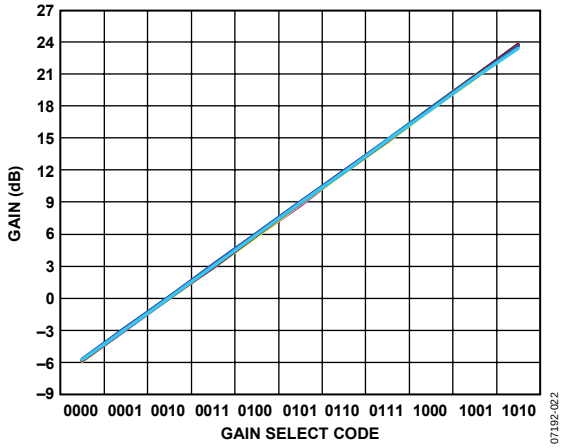


Figure 22. Gain vs. Gain Select Code

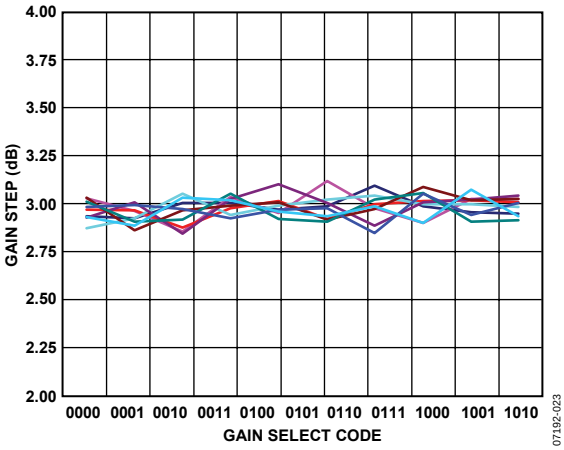


Figure 23. Gain Step vs. Gain Code

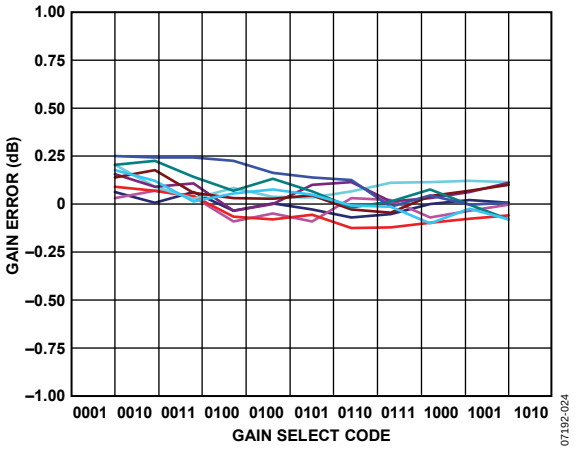


Figure 24. Gain Error vs. Gain Select Code

TBD

Figure 25

TBD

Figure 26

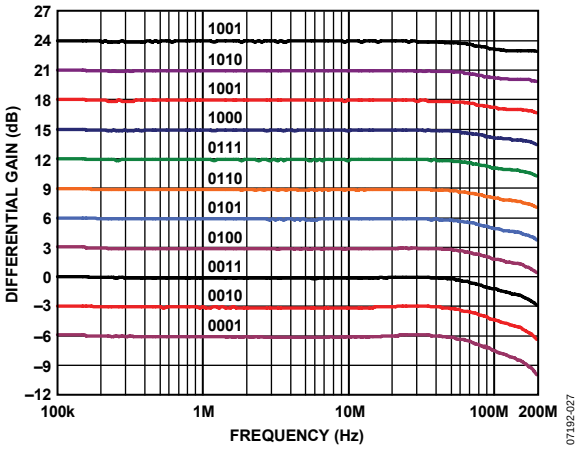


Figure 27. Frequency Response at V_S = 3.3 V for all Codes

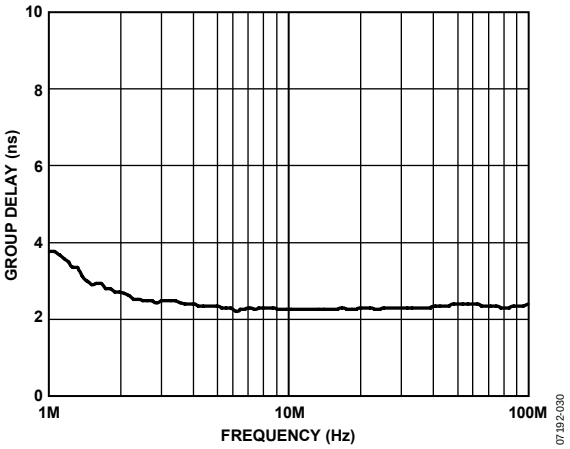


Figure 30. Group Delay vs. Frequency

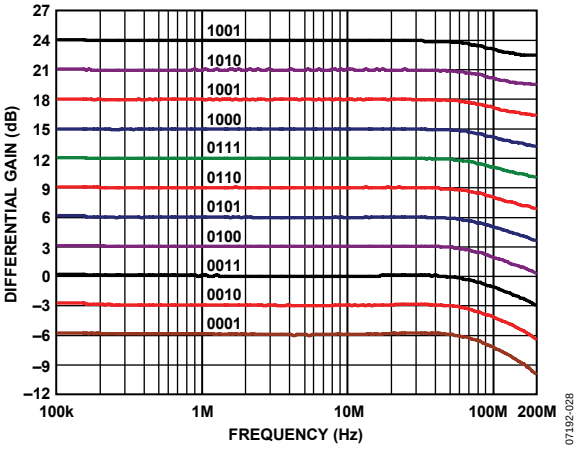


Figure 28. Frequency Response at V_S = 5 V for All Codes

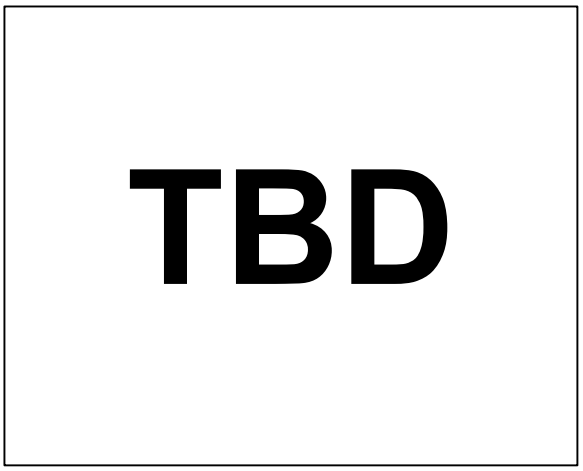


Figure 31.

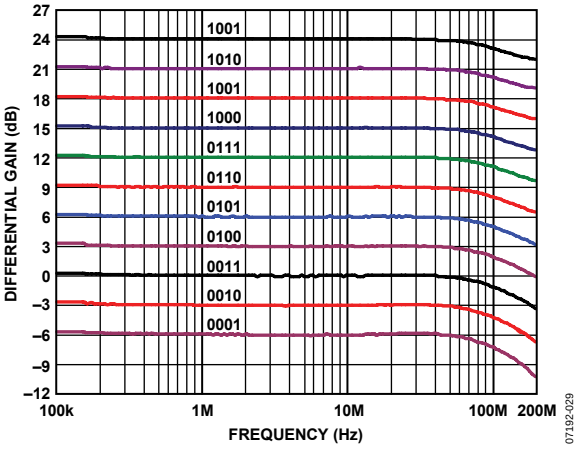


Figure 29. Frequency Response at V_S = ±5 V for All Codes

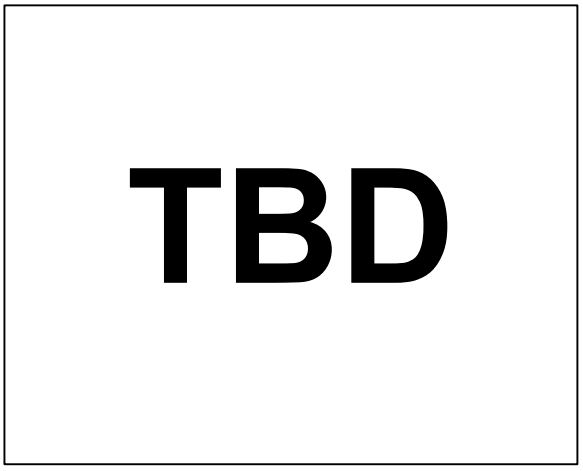


Figure 32.

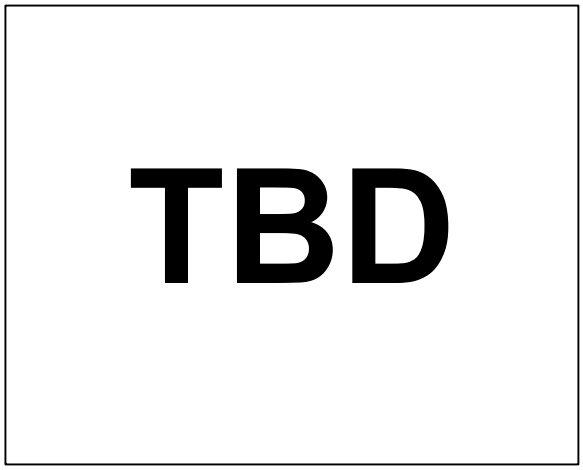


Figure 33.

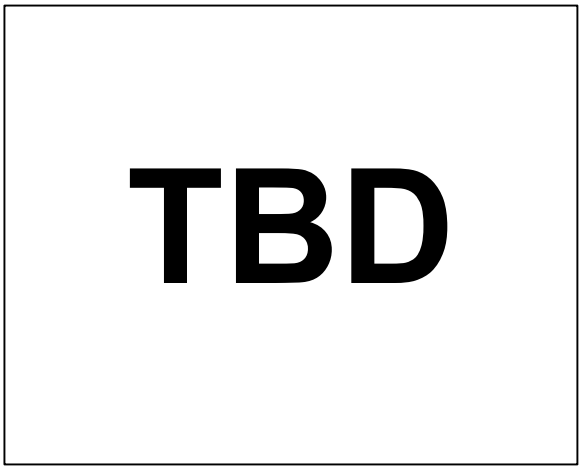


Figure 36.

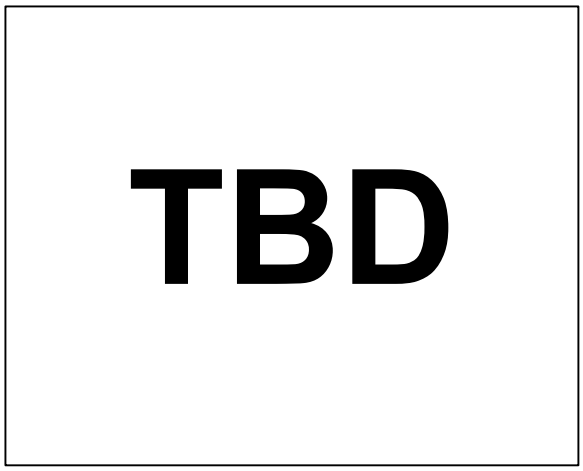


Figure 34.

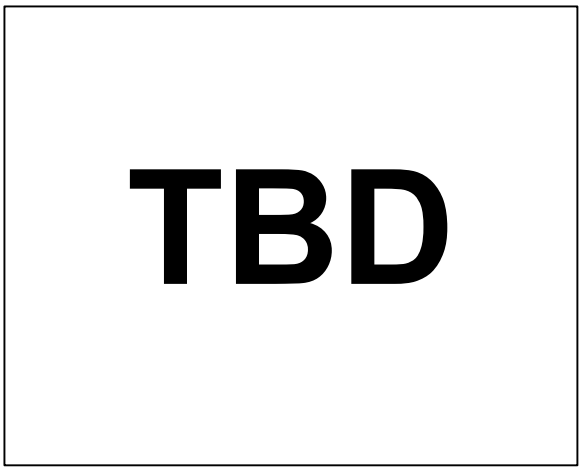


Figure 37.

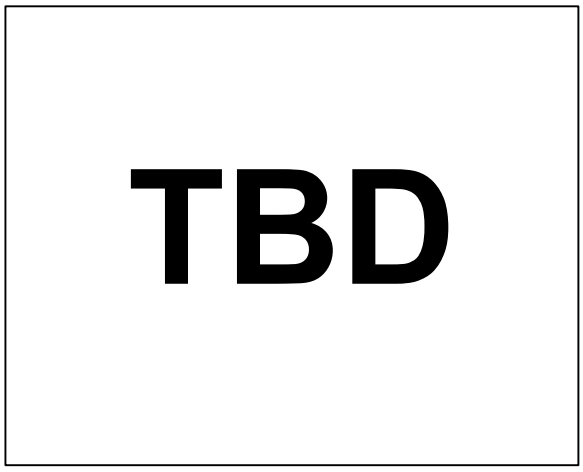


Figure 35.

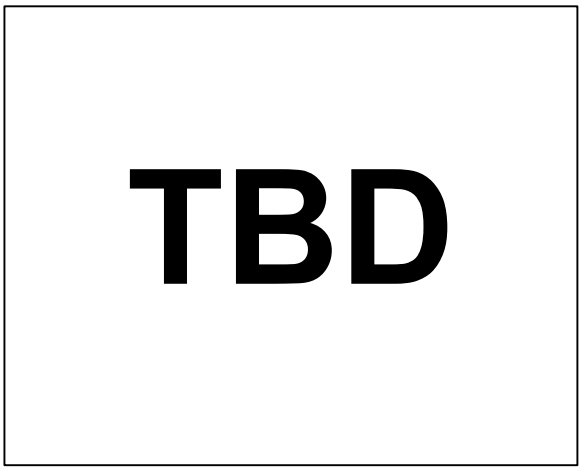


Figure 38.

TBD

Figure 39.

TBD

Figure 40.

TBD

Figure 41.

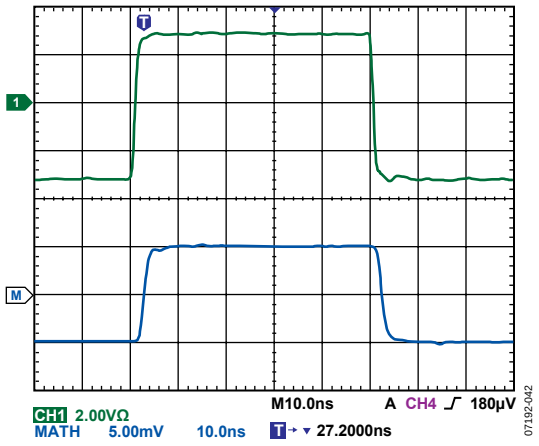


Figure 42. Small Signal Pulse Response

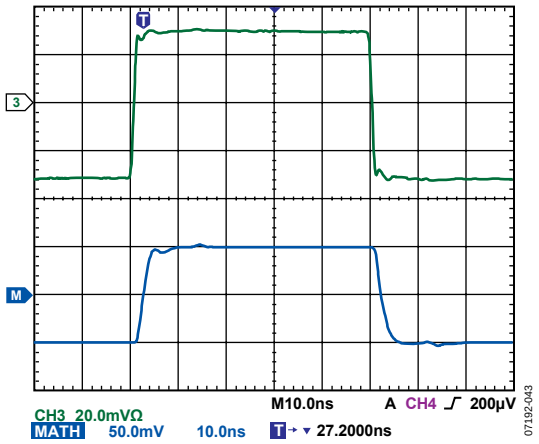


Figure 43. Large Signal Pulse Response

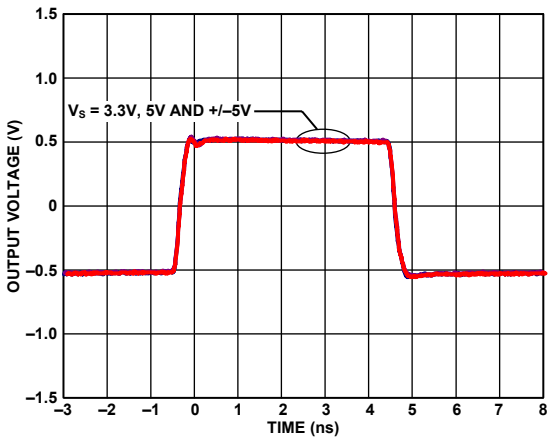


Figure 44. Large Signal Pulse Response for Various Values of Supply Voltage

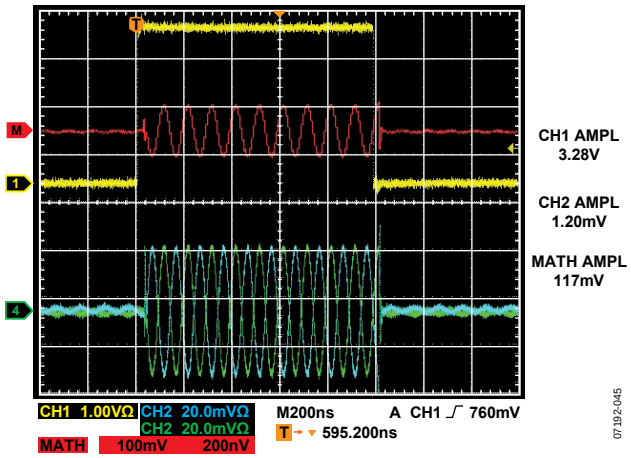


Figure 45. Gain Response

TBD

Figure 46.

TBD

Figure 47.

TBD

Figure 48.

TBD

Figure 49.

Figure 50.

THEORY OF OPERATION

INTRODUCTION

The AD8260 is a self-contained transceiver intended for analog communications using a power line as the media. It includes a high current driver usable as a transmitter, and a low noise, digitally programmable variable gain amplifier (DGA) useable as a receiver (see Figure 51). A high frequency current-feedback preamplifier is the interface to the DGA and is user configured for gains greater than 6 dB. Combined, the VGA and preamplifier are useable from dc to frequencies as high as 80 MHz, with a −3 dB bandwidth of 180 MHz.

The small signal −3 dB bandwidth of the driver amplifier is 155 MHz and the large signal BW is >115 MHz, even when driving a 50 Ω load.

The device is fabricated on the Analog Devices, Inc., high speed (eXtra Fast Complementary Bipolar) XFCB process. The PrA + DGA feature low dc offset voltage and a nominal gain range of −6 dB to +24 dB, a 30 dB gain span and a differential output for ADC driving. The power consumption is 93 mW with a single 3.3 V supply. The supply current is typically ~28 mA when all circuits in the device are active. During normal usage, either the driver amplifier is on or the PrA + DGA is on and, therefore, the power consumption in general is less than 28 mA. The AD8260 gain is programmed through a parallel interface (four bits). Figure 51 shows the circuit block diagram of the AD8260, which also shows the envisioned external connections for the DAC, ADC, and power-line bus interface. The diagram shows the connections for single 3.3 V supply operation; if a dual supply is available, the VMID generator can be shut down and Pin VMDI, Pin VMDO, and Pin VOCM are grounded. Note that Pin VNCM functions as the negative supply for the bias and VMID cells, plus the logic interfaces, and should always be tied to ground.

For optimal dynamic range, it is important that the inputs and outputs to both the driver amplifier and the preamplifier and the DGA output amplifier are ac-coupled in a single-supply application. In Figure 51, the DAC and ADC are presumed to operate on a 1.8 V or 3.3 V supply with a corresponding limited output and input swing. The DAC outputs are currents that point down and generate a voltage in the 50 Ω resistors that are connected to ground. The maximum voltage with a peak output current of 15 mA is 0.75 V; if a DAC with a 20 mA peak current is used, then the maximum voltage is 1 V per side for a differential input signal of 2 V p-p.

The driver amplifier supports a 3 V p-p output swing on a 3.3 V supply. Because of its gain of 1.5, the maximum input swing is 2 V p-p. The corresponding output swing for the DGA is 2.4 V p-p differential; the input to the preamplifier can be a maximum of 0.6 V p-p.

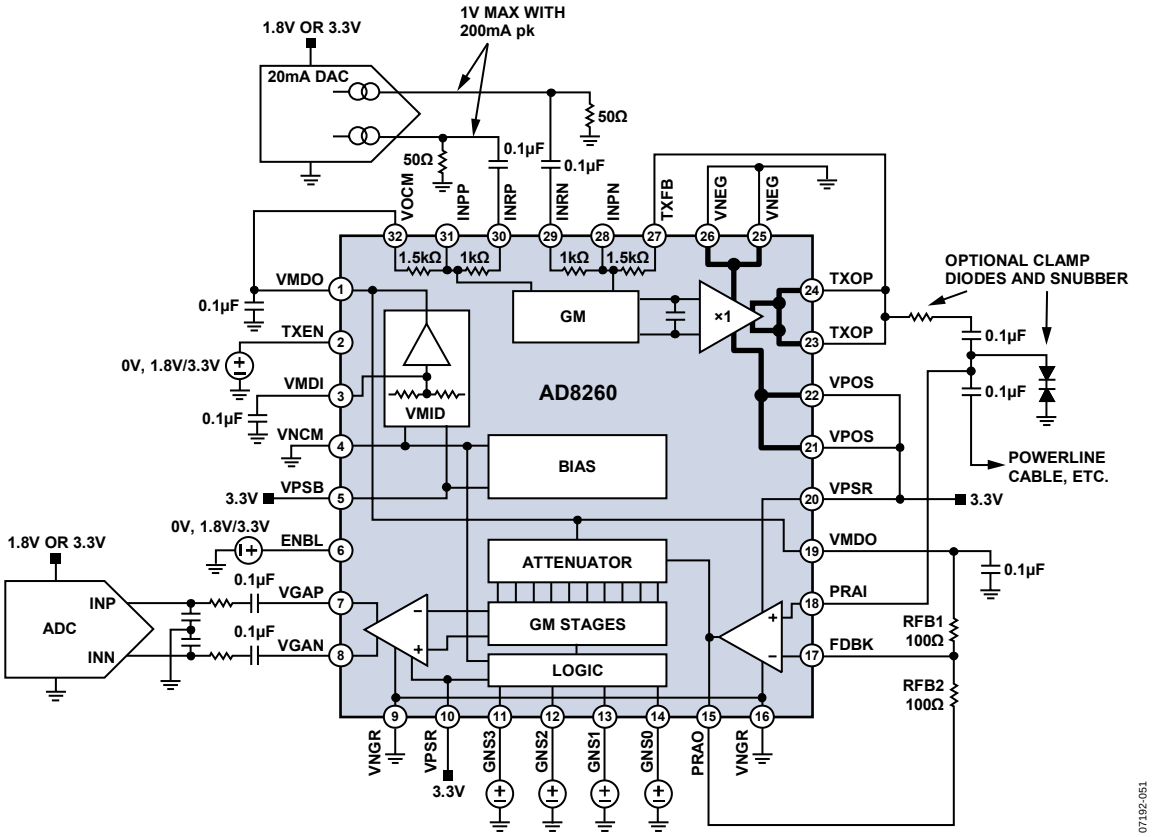


Figure 51 Block diagram and pinout

HIGH CURRENT DRIVER AMPLIFIER

The high current driver amplifier can deliver very large output currents suitable for driving complex impedances, such as a power line, a 50 Ω line, or coaxial cable. The amplifier is designed to be driven differentially from a DAC, as shown in Figure 51. The differential input signal is amplified by 1.5× and produces a 2.25 V p-p single-ended output signal from a 1.5 V p-p input signal. A DAC with a 15 mA maximum output signal into a 50 Ω load provides a suitable input voltage. A DAC whose output is 20 mA produces an output swing of 3 V p-p. Note that the output voltage swing limit when using a 3.3 V supply is a maximum of 3 V p-p and distorts severely if increased further. The recommended output swing to optimize distortion is 2 V p-p using a 3.3 V supply. For higher supply voltages, such as +5 V or ±5 V, a correspondingly larger swing can be accommodated.

Because of the supply-limited output swing, the input level should not exceed that level, which results in the optimum distortion. For example, a 20 mA DAC can be used with resistors less than 50 Ω in value, or the gain reduced by connecting external resistors in parallel with the internal 1 kΩ and 1.5 kΩ resistors between Pin 27, Pin 28, and Pin 29, or between Pin 27, Pin 28, and Pin 29. Note that the noise is reduced this way because the gain setting resistors are the primary noise sources of the high current driver amplifier.

The output-referred noise is 14 nV/√Hz, of which 11 nV/√Hz is due to the gain setting resistors. Matching of the gain setting resistors is important for good common-mode rejection and the accuracy of the differential gain. If external resistors are used, their accuracy should be at least ±1%. How low the resistor values can be is primarily determined by the quality of the ac ground at Node VOCM. As the gain setting resistors decrease in value, the dynamic current increases and the quality of the decoupling caps needs to increase correspondingly.

PRECAUTIONS TO BE OBSERVED DURING DESIGN

When the high current driver-amplifier is disabled, the gain setting resistors provide a signal path from input to output. To prevent inadvertent DAC signals from being transmitted when the preamplifier and DGA are enabled, the DAC in Figure 51 must have no output signal.

VMID BUFFER

The VMID buffer is a dc bias source for the high current driver-amplifier and cannot accommodate large dynamic currents. The function of the external decoupling capacitors shown at Pin 1 and Pin 19 in Figure 51 is to divert high values of current.

When operating with dual power supplies, the buffer is disabled by connecting Pin VMDI, Pin VOCM, and Pin VMDO to ground. Because of the logic decoder in the DGA (GNSx inputs), all the positive supplies need to be at least 3.3 V. The negative supplies are the same magnitude but are opposite polarity of the positive supplies, that is, −3.3 V when VPOS, VPSB, and VPSR are +3.3 V.

PREAMPLIFIER

The AD8260 includes an uncommitted current feedback op amp that is used as a preamplifier to buffer the resistive attenuator of the DGA. The gain is adjusted by the user, with external resistors. The preamplifier is characterized with a noninverting gain of 6 dB (2×) and both gain resistor values of 100 Ω. The preamplifier gain can be increased using different gain ratios of R_{FB1} and R_{FB2}, trading off bandwidth and offset voltage. The value of R_{FB1} + R_{FB2} should be ≥200 Ω to maintain low distortion. R_{FB2} should be ≥100 Ω because it, and an internal compensation capacitor, determine the −3 dB bandwidth of the amplifier. Smaller resistor values may compromise preamplifier stability. Because the AD8260 is internally dc-coupled, larger preamplifier gains increase the offset voltage. The circuit contains an internal bias resistor and some offset compensation; however, if a lower value of offset voltage is required, it can be compensated by connecting a resistor between the INPN pin and the supply voltage. If the offset is negative, the resistor value connects to the negative supply; otherwise, it connects to the positive supply.

For larger gains, the overall noise is reduced if a low value of RFB1 is selected. For values of RFB1 = 20 Ω and RFB2 = 301 Ω, the preamplifier gain is 16× (24.1 dB) and the input-referred noise is about 1.5 nV/√Hz. For this value of gain, the overall gain range increases by 18 dB so that the gain range is 12 dB to 42 dB.

PREAMPLIFIER NOISE

The total input-referred voltage and current noise of the positive input of the preamplifier is about 2.4 nV/√Hz and 5 pA/√Hz, respectively. The DGA output-referred noise is about 25 nV/√Hz at low gains and 39 nV/√Hz at the highest gain. The 25 nV/√Hz divided by the DGA fixed gain of 8× results in 3.12 nV/√Hz referred to the DGA input. Note that this value includes the noise of the DGA gain setting resistors as well. If this voltage is divided by the preamplifier gain of 2×, the DGA noise referred all the way to the preamplifier input is about 1.56 nV/√Hz. From this, it can be determined that the preamplifier, including the 100 Ω gain setting resistors, contributes about 1.8 nV/√Hz. The two 100 Ω resistors contribute 1.29 nV/√Hz each at the output of the preamplifier and 0.9 nV/√Hz referred to the input. With the gain resistor noise subtracted, the preamplifier noise alone is about 1.6 nV/√Hz.

The following equation shows the calculation that determines the output-referred noise at maximum gain (24 dB or 16×):

$$e_{n-out} = \sqrt{\left(\sqrt{4kTRB} \times A_t\right)^2 + (e_{n-\mathrm{Pr}A} \times A_t)^2 + (i_{n-\mathrm{Pr}A} \times R_S)^2 + (e_{n-RFB1} \times \frac{RFB2}{RFB1} \times A_{VGA})^2 + (e_{n-RFB2} \times A_{VGA})^2 + (e_{n-VGA} \times A_{VGA})^2} \quad (1)$$

where:
A_t is the total gain from preamplifier input to VGA output.
R_S is the source resistance.
$e_{n\text{-}PrA}$ is the input-referred voltage noise of preamplifier.
$i_{n\text{-}PrA}$ is the current noise of preamplifier at the PRAI pin.
$e_{n\text{-}RFB1}$ is the voltage noise of R_{FB1}.
$e_{n\text{-}RFB2}$ is the voltage noise of R_{FB2}.
$e_{n\text{-}VGA}$ is the input-referred voltage noise of DGA (low gain output-referred noise divided by a fixed gain of 8×).

Assuming $R_S = 0$, $R_{FB1} = R_{FB2} = 100\ \Omega$, $A_t = 16$, and $A_{VGA} = 8\times$, the noise simplifies to

$$e_{n-out} = \sqrt{(1.6\times16)^2 + 2\,(1.29\times8)^2 + (3.12\times8)^2} = 39\ \text{nV}/\sqrt{\text{Hz}} \quad (2)$$

Taking this result and dividing it by 16 gives the total input-referred noise with a short-circuited input as 2.4 nV/√Hz. When the preamplifier is used in the inverting configuration with the same $R_{FB1} = R_{FB2} = 100\ \Omega$ in the previous example, then $e_{n\text{-}out}$ does not change; however, because the gain decreases by 6 dB, the input-referred noise increases by a factor-of-2 to about 4.8 nV/√Hz. The reason for this is that the noise gain to the DGA output of all the noise generators stays the same, but the inverting-feedback gain is −1× compared to the +2× in the noninverting configuration. This increases the input-referred noise by 2.

DGA

Referring to Figure 51, the signal path consists of a 30 dB programmable attenuator followed by a fixed gain amplifier of 18 dB for a total DGA gain range of −12 dB to +18 dB. With the preamplifier configured for a gain of 6 dB, the composite gain range is −6 dB to +24 dB from single-ended preamplifier input to a differential DGA output.

The DGA plus preamplifier with 6 dB of gain implements the following gain law:

$$Gain(\text{dB}) = \left[3.01\frac{dB}{Code}\times Code\right] + ICPT(\text{dB})$$

where:
ICPT is the nominal intercept, −9 dB.
Code values are decimal from 1 to 11.

The ICPT increases as the gain of the preamplifier is increased. For example, if the gain of the preamplifier is increased by 6 dB, then ICPT increase to −3 dB.

GAIN CONTROL

To change the gain, the desired four bits are programmed on Pin GNS0 to Pin GNS3, where GNS0 is the LSB (D0) and GNS3 is the MSB (D3). The states Decimal 0 and Decimal 12 through Decimal 15 disable the PrA and DGA (see Table 4).

Table 4. Gain Control Logic Table

D3	D2	D1	D0	Function	Comments
0	0	0	0	Disable	PrA + DGA powered down
0	0	0	1	−6	The numbers in the function column are composite gain values in dB for the corresponding code, when the preamplifier gain is 6 dB. For other values of preamplifier gain the gain is amended accordingly; for example, if the preamplifier gain = 0 dB, the gain values diminish by 6 dB. When using the DGA single-endedly, the composite gain is diminished by 6 dB.
0	0	1	0	−3	
0	0	1	1	0	
0	1	0	0	3	
0	1	0	1	6	
0	1	1	0	9	
0	1	1	1	12	
1	0	0	0	15	
1	0	0	1	18	
1	0	1	0	21	
1	0	1	1	24	
1	1	0	0	Disable	PrA + DGA powered down
1	1	0	1		
1	1	1	0		
1	1	1	1		

OUTPUT STAGE

The gain of the voltage feedback output stage is fixed at 18 dB, and inaccessible to the user. Otherwise, it is similar to the preamplifier in speed and bandwidth. The overall −3 dB bandwidth of the PrA + DGA combination is 180 MHz.

ATTENUATOR

The input resistance of the VGA attenuator is nominally 265 Ω. Assuming that the default preamplifier feedback network of R_{FB1} and R_{FB2} is 200 Ω, the effective preamplifier load is about 114 Ω. The attenuator is composed of ten 3.01 dB sections for a total attenuation span of −30.10 dB. Following the attenuator is a fixed gain amplifier with 18 dB (8×) gain. Because of this relatively low gain, the output offset is less than 20 mV over the operating temperature range; the offset is largest at maximum gain because the preamplifier offset is amplified. The VMDO pin defines the common-mode reference for the input and output. The voltage at VMID is half the supply voltage for single-supply operation, and 0 V when dual supplies are used.

SINGLE-SUPPLY OPERATION AND AC COUPLING

When operating the AD8260 from a single supply, there are two bias options for VMDO.

- Use an external low impedance midpoint reference at Pin VMDO and pull VMDI to VNCM to shut down the VMID buffer.
- Use the internal VMID buffer as shown in Figure 51.

In both cases, decoupling capacitors need to be connected to Pin VMDO to absorb the dynamic currents.

During single-supply operation, the preamplifier input is normally ac-coupled. An internal bias resistor (nominally 1 k Ω) connected between PRAI and VMDO provides bias to the

preamplifier input pin. A 50 Ω resistor connected between Pin PRAI and Pin VMDO, in parallel with the internal 1 kΩ, serves as a termination resistor, with a composite value of about 48 Ω impedance. The VGA input is biased through the attenuator network and the voltage at Pin VMDO. When active, the VMID buffer provides the needed bias currents. When the buffer is disabled, an external voltage is required at Pin VMDO to provide the bias currents. For example, for a single 5 V application, a reference such as the ADR43 and a stable op amp provide an adequate VMDO source.

POWER UP/DOWN SEQUENCE

For glitch-free power-up operation, the following power-up and power-down sequence is recommended:

1. Enable the bias by pulling the ENBL pin high. Maintain GNS0 to GNS3 and TXEN at ground.
2. It is assumed that after the part wakes up from sleep mode, the receive section (PrA + DGA) needs to be active first to listen to any signals, and the driver needs to be off. Therefore, the gain code should be set to 0001 (−6 dB of gain) first and then the gain adjusted as needed. Note that any code besides 1 to 11 (binary) disables the receive section (see Table 4). During receive, it is also important that the DAC that provides the signal for the high-current driver must be disabled to avoid interfering with the received signal.
3. After receive, presumably data needs to be transmitted via the high current driver amplifier. At this point, the DAC should still be off. Pull pin TXEN high and allow the high current driver to settle. Enable the DAC. Although the preamplifier and DGA can remain enabled during the previous sequence, there may be significant preamplifier overdrive, and it is best that the receiver be disabled during transmitting.
4. Pull Pin ENBL low to disable the preamplifier. To achieve the specified sleep current, all logic pins must be pulled low as well.

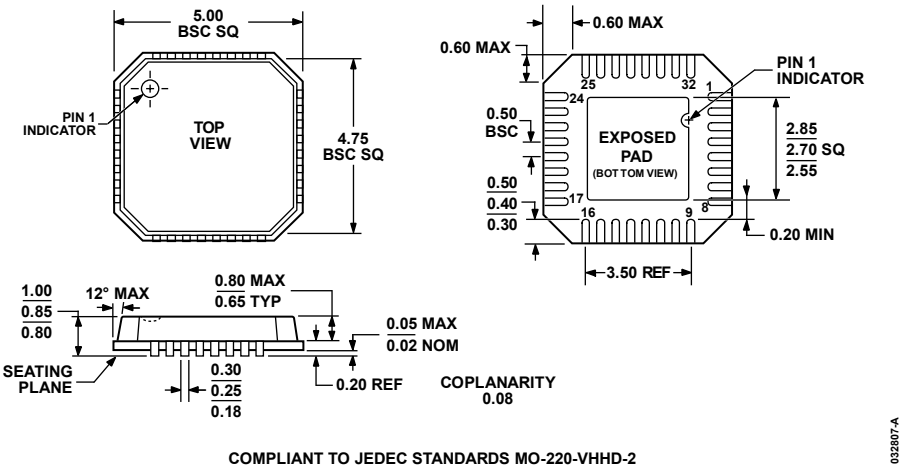
LOGIC INTERFACES

All logic pins use the same interfaces and, therefore, have the same behavior and thresholds. The interface contains a Schmitt trigger type input with a threshold at about 1.1 V and a hysteresis of ±0.2 V.

Therefore, the logic low is between ground and 0.8 V, and logic high is from 1.4 V to VPOS. Because the threshold is so low, the logic interfaces can be driven directly from 1.8 V or 3.3 V CMOS.

The input bias current is nominally 300 nA when the applied voltage is 3.3 V and 0 V when grounded.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 52 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD8260ACPZ-R7[1]	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-8
AD8260ACPZ-RL[1]	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-8
AD8260ACPZ-WP[1]	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-8

[1] Z = RoHS Compliant Part.

PR07192-0-1/08(PrA)